Code No: R1622023 **R16** SET - 1

II B. Tech II Semester Regular/Supplementary Examinations, November - 2020
SWITCHING THEORY AND LOGIC DESIGN
(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Convert the number 612_8 with the given radix to decimal (2M)
   b) Draw the K map for 4 variables. (2M)
   c) Draw the circuit diagram of a full-subtractor using NOR gates. (3M)
   d) Compare PLDs with PLAs (3M)
   e) Distinguish between combinational logic and sequential logic (2M)
   f) What is Finite state machine? (2M)

PART -B

2. a) Convert the following expressions into sum of products and product of sum. (7M)
      1. (AB+C)(B+C'D)
      2. X'+X(X+Y')(Y+Z')
   b) Simplify the following function and implement it with NAND gates (7M)
      F= (B'+D')(A'+C'+D)(A+B'+C'+D)(A'+B+C'+D')

3. a) Simplify the following three variable expressions using Boolean algebra: $Y = \sum m(1,3,5,7)$. (7M)
   b) Explain the procedure of minimization of switching function using tabular method with example (7M)

4. a) Perform the realization of half adder and full adder using decoders and logic gates. (7M)
   b) Using 8 to 1 multiplexer, realize the Boolean function: (7M)
      $T = f(w, x, y, z) = \sum(0, 1, 2, 4, 5, 7, 8, 9, 12, 13)$

5. a) Implement the following Boolean functions using PAL F1 (X, Y, Z) = $\sum$ (1, 2, 4, 6) F2 (X, Y, Z) = $\sum$ (0, 1, 6, 7) F3 (X, Y, Z) = $\sum$ (2, 6) (7M)
   b) Discuss the merits & demerits of PROM, PAL, PLA (7M)

6. a) What is the procedure to Conversion from one flip-flop to other flip-flop? Convert JK Flip Flop to D Flip Flop using conversion logic. (7M)
   b) Design a 4-bit ring counter using T-flipflops and draw the circuit diagram and timing diagram. (7M)

7. a) Define the following (7M)
      i. State ii. State diagram iii. State table
   b) With an example explain the reduction of state table and state assignment (7M)

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