Code No: R1622023 **R16** SET - 1

II B. Tech II Semester Supplementary Examinations, April - 2021
SWITCHING THEORY AND LOGIC DESIGN
(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1.	a)	What is self complement code? mention some self complement codes	(2M)
	b)	What are the advantages of K-map?	(3M)
	c)	What is Multiplexer?	(2M)
	d)	What is difference between a PLA and ROM?	(3M)
	e)	Define flip-flop?	(2M)
	f)	Explain the meaning of the term 'state equivalence'	(2M)

PART -B

2.	a)	Deduce X from the following? (i) $(BA0.C)_{16} = (X)_8$ (ii) $(10101100)_2 = (X)_{16}$ (iii) $(FFE.C)_{16}=(X)2$ (iv) $(7562)_8 = (X)2$	(8M)
	b)	Explain about non-weighted codes	(6M)
3.	a)	Simplify the following Boolean expressions to a minimum number of literals i)ABC+A'B+ABC' ii)x'yz +xz iii) (x +y)'(x' + y')	(7M)
	b)	Difference between K map and Tubular method	(7M)
4.	a)	Implement the following Boolean function with a decoder (a) $F(A, B, C, D) = \sum(1, 2, 5, 8, 6, 10,12,14)$ (b) $F(A, B, C, D) = \sum(1, 2, 5,6, 12)$	(7M)
	b)	What is necessity of priority encoder? Explain about 8 to 3 priority encoder.	(7M)
5.		Design a BCD to seven segment decoder using (a) PAL (b) PLA	(7+7M)
6.	a)	With the aid of external logic, convert D type flip-flop to a SR flip-flop	(7M)
	b)	What is a shift register? Draw the block diagram and timing diagram of a shift register that shows the serial transfer of information from register A to register B.	(7M)
7.	a)	What is Finite state machine and explain its capabilities	(7M)
	b)	Draw a state diagrams of a sequence detector which can detect 011	(7M)

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