Code No: R193104B **R19** **SET - 1**

III B. Tech I Semester Supplementary Examinations, June/July-2022

DIGITAL SYSTEM DESIGN USING HDL

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) Write down the step by step approach of FPGA design process on XILINX environment. [8M]
   b) Draw and explain the basic architecture of FPGA. [7M]

(OR)

2. a) With the help of example explain the structure of a Verilog test bench file. [8M]
   b) Explain three different methods of modeling in describing a digital system in Verilog with examples. [7M]

UNIT-II

3. a) Give the syntax for a net declaration? Explain the different kind of nets that belong to the net data type. [8M]
   b) What are the different arithmetic operators in Verilog? Write a Verilog code for arithmetic operations on two eight bit vectors. [7M]

(OR)

4. a) List out the five different kinds of variable data types. Explain each one with declaration. [8M]
   b) Construct a primitive calculator to add, subtract, multiply and divide two 4-bit numbers on the Basys3 board in Verilog. [7M]

UNIT-III

5. a) Distinguish between combinational and sequential circuits. List some applications of sequential circuits. [8M]
   b) Implement the Verilog HDL source code and logic diagram for 1-bit full adder using data flow style. [7M]

(OR)

6. a) Draw the schematic circuit of a D flip flop with negative edge triggering using NAND gates. Give its truth table and explain its operation. [8M]
   b) Explain the modeling approach for static RAM memory using Verilog HDL. Modeling approach consists of design and implementation. [7M]

UNIT-IV

7. a) List the basic types of shift registers in terms of data movement with diagrams? Also discuss the applications of shift registers. [8M]
   b) Write a Verilog description of the 8-bit parallel in/parallel out shift register for multiplication and division operations. [7M]

(OR)

8. a) Write the design steps of synchronous counters with suitable examples. [8M]
   b) Implement the Verilog HDL module of N-bit Synchronous Up/Down counter. [7M]

UNIT-V

9. a) What is a translator? Implement translator on the Basys3 Board in Verilog. [8M]
   b) Briefly discuss about Air Freshener Dispenser application with neat diagram. [7M]

(OR)

10. a) Define UART. Explain the working principle of UART. [8M]
    b) Explain the difference between I2C and SPI communication interface. [7M]

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