Code No: R203104Q **R20** SET - 1

III B. Tech I Semester Regular Examinations, Dec/Jan -2022-23

DIGITAL LOGIC DESIGN

(Common to CSE, IT)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) i) Convert $(8B7.A4)_{16}$ toits binary equivalent. [7M]
   ii) Convert $(714.36)_8$ to its hexadecimal equivalent.
   b) Encode the binary word 10111 into 9 bit hamming code for odd parity. [7M]

(OR)

2. a) i) What are the universal gates? Why they are called as universal gates? Discuss with the figures. [7M]
   ii) Draw the Logic diagram and explain the truth table of EX-OR and EX-NOR gates.
   b) i) State and prove De-morgan theorems. [7M]
   ii) Reduce the following Boolean Expression:
   AB+ABC+AB(D+E).

UNIT-II

3. a) Simplify the following function using K-Map: [7M]
   $F(A,B,C,D)=\sum(0,2,3,8,10,11,12,14)$
   b) Design a full adder by using two half adders. [7M]

(OR)

4. a) Simplify the following function using K-Map: [7M]
   $F(A,B,C,D,E)= \Pi(0,1,6,7,8,9,21,22,23,29,31)$
   b) Implement Carry look-a-head adder circuit and explain its operation briefly. [7M]

UNIT-III

5. a) Implement the following Boolean functions using PROM: [7M]
   $F_1(A_2,A_1,A_0)=\sum(0,1,2)$, $F_2(A_2,A_1,A_0)=\sum(3,4,5)$, $F_3(A_2,A_1,A_0)=\sum(2,4,6)$
   b) Draw the pin diagram and obtain the truth table of IC 7485? [7M]

(OR)

6. a) Design a 4 to 2 priority encoder. [7M]
   b) Implement the following Boolean function using 4:1 Mux: [7M]
   $F(A,B,C,D)=\sum(0,2,3,6,11,13,15)$

UNIT-IV

7. a) What is a Flip flop? Explain the SR flip flop with the help of logic diagram, truth table and excitation table. [7M]
   b) Design a 3 bit Synchronous Counter. [7M]

(OR)

8. a) Convert SR Flip flop into JK flip flop. [7M]
   b) What is a register? Explain the operation of Parallel In Serial Out shift register (PISO). [7M]

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UNIT-V

9. a) Explain the differences between Mealy and Moore Machine. [7M]
   b) What is a Finite State Machine? Explain the capabilities and limitations of Finite State Machine. [7M]

(OR)

10. a) Explain the designing steps to convert Mealy machine to Moore machine. [7M]
    b) Design a finite state machine which can detect the sequence 0010. [7M]

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Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1. a) i) If $(211)_{\mathbf{x}}=(152)_8$,find X. [7M]
   ii) Convert $(24.95)_{10}$ to its binary equivalent.
   b) Encode the binary word 11001 into 9 bit hamming code for even parity. [7M]

(OR)

2. a) i) Implement an EX-OR gate logic using NOR gates. [7M]
   ii) Implement an OR gate logic using NOR gates.
   b) i) Convert the given SOP to standard SOP: [7M]
   A+BC
   ii) Reduce the following Boolean Expression:
   $XY+XYZ+XYZ^1+X^1YZ$

UNIT-II

3. a) Simplify the following function using K-Map: [7M]
   $F(A,B,C,D,E)=\sum(0,2,4,7,8,10,12,16,18,20,23,24,25,26,27,28)$
   b) Design a full subtractor by using two half subtractors. [7M]

(OR)

4. a) Simplify the following function using K-Map: [7M]
   $F(A,B,C,D)= \Pi(0,1,2,3,5,7,11)$
   b) Implement a 4 bit Binary to Gray code converter. [7M]

UNIT-III

5. a) Implement the following Boolean functions using PLA: [7M]
   $A(X,Y,Z)=\sum(1,2,4,6)$, $B(X,Y,Z)=\sum(0,1,6,7)$, $C(X,Y,Z)=\sum(2,6)$
   b) Draw the pin diagram and obtain the truth table of IC 74154. [7M]

(OR)

6. a) What is decoder? Construct a 4:16 decoder with two 3:8 decoders. [7M]
   b) Implement the following Boolean function using 8:1 Mux: [7M]
   $F(A,B,C,D)=\Pi(1,5,8,9,12,15)$

UNIT-IV

7. a) What is Race around condition? Explain the JK flip flop with the help of logic diagram, truth table and excitation table. [7M]
   b) Design a 3 bit Asynchronous Counter. [7M]

(OR)

8. a) Convert JK Flip flop into SR flip flop. [7M]
   b) What is a register? Explain the operation of Universal Shift Register. [7M]

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UNIT-V

9. a) Explain the designing steps to convert Mealy machine to Moore machine. [7M]
   b) Explain the capabilities and limitations of Finite State Machine. [7M]

(OR)

10. a) Explain the Mealy and Moore Machines with neat figures. [7M]
    b) Design a finite state machine which can detect the sequence 0111. [7M]

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DIGITAL LOGIC DESIGN

(Common to CSE, IT)

Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1. a) i) Find the 2's complement of $(110101)_2$. [7M]
   ii) Find the 8's complement of $(346510)_8$.
   iii) Convert $(1011011)_2$ to its Gray code equivalent.
   b) Determine which bit is having error in the received 7 bit even parity hamming code, 0100011. [7M]

(OR)

2. a) i) Implement an EX-NOR gate logic using NOR gates. [7M]
   ii) Implement an AND gate logic using NOR gates.
   b) i) Convert the given SOP to standard SOP: [7M]
   $XY+X^1Z+YZ$
   ii) Reduce the following Boolean Expression:
   $A(A+B)$

UNIT-II

3. a) Simplify the following 5 Variable function using K-Map: [7M]
   $F=\sum(0,2,3,5,7,8,10,11,14,15,16,18,24,26,27,29,30,31)$
   b) Design a 4 bit adder-subtractor circuit and explain its operation. [7M]

(OR)

4. a) Simplify the following function using Tabular method: [7M]
   $F(A,B,C,D)=\sum(0,2,3,6,7,8,10,12,13)$
   b) Implement a 4 bit Gray to Binary code converter. [7M]

UNIT-III

5. a) Implement the following Boolean functions using PAL: [7M]
   $A(X,Y,Z)=\sum(1,2,4,6)$, $B(X,Y,Z)=\sum(0,1,6,7)$, $C(X,Y,Z)=\sum(2,6)$
   b) Implement a 4-bit digital comparator and explain its operation. [7M]

(OR)

6. a) What is a multiplexer? Construct a 8:1multiplexer with two 4:1multiplexers. [7M]
   b) Implement the following Boolean function using 4:1 Mux: [7M]
   $F(A,B,C,D)=\sum(1,2,5,8,9,12,14)$

UNIT-IV

7. a) What is a Flip flop? Explain the D flip flop with the help of logic diagram, truth table and excitation table. [7M]
   b) Design a 4 bit Johnson counter. [7M]

(OR)

8. a) Convert D Flip flop into T flip flop. [7M]
   b) Design a 4 bit Serial In Serial Out (SISO)– shift left register and explain its operation. [7M]

UNIT-V

9. a) What is a Finite State Machine? Explain the capabilities and limitations of Finite State Machine? [7M]
   b) Explain the differences between Mealy and Moore Machine? [7M]

(OR)

10. a) Design a finite state machine which can detect the sequence 0111. [7M]
    b) Explain the designing steps to convert Moore machine to Mealy machine? [7M]

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DIGITAL LOGIC DESIGN

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Time: 3 hours Max. Marks: 70

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
*****

UNIT-I

1. a) i) Find the 10's complement of $(278600)_{10}$ [7M]
   ii) Find the 16's complement of $(34CEDA)_{16}$
   iii) Convert given Gray code (1100110) to its Binary code equivalent.
   b) Determine which bit is having error in the received 9 bit odd parity hamming code, 101101101. [7M]

(OR)

2. a) i) Implement an EX-OR gate logic using NAND gates. [7M]
   ii) Implement an AND gate logic using NAND gates.
   b) i) Convert the given POS to standard POS: [7M]
   (X+Y)(Y+Z)(X+Z)
   ii) Draw the pin diagram and obtain the truth table of IC 7400.

UNIT-II

3. a) Simplify the following 6 Variable function using K-Map: [7M]
   F=∑(0,5,7,8,9,12,13,23,24,25,28,29,37,40,42,44,46,55,56,57,60,61)
   b) Implement a 4 bit BCD to Binary code converter. [7M]

(OR)

4. a) Simplify the following function using Tabular method: [7M]
   F(A,B,C,D)= Π(2,4,5,9,12,13)
   b) Implement a 4 bit Binary to BCD code converter. [7M]

UNIT-III

5. a) Distinguish between PROM, PLA and PAL. [7M]
   b) Implement a seven segment decoder and explain its operation. [7M]

(OR)

6. a) What is a de-multiplexer? Construct a 1:8 de-multiplexer with two 1:4 de-multiplexers. [7M]
   b) Implement the following Boolean function using 8:1 Mux: [7M]
   F(A,B,C,D)=Π(0,2,3,5,7,11,14,15)

UNIT-IV

7. a) What is a Flip flop? Explain the T flip flop with the help of logic diagram, truth table and excitation table. [7M]
   b) Design a 4 bit Ring counter. [7M]

(OR)

8. a) Convert T Flip flop into D flip flop. [7M]
   b) Design a 4 bit Serial In Serial Out (SISO)– shift right register and explain its operation. [7M]

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UNIT-V

9. a) What is a Finite State Machine? Explain the capabilities and limitations of Finite State Machine. [7M]
   b) Discuss the process to convert Moore machine to Mealy machine? [7M]

(OR)

10. a) Design a finite state machine which can detect the sequence 0010? [7M]
    b) Differentiate the mealy machine and moore machine. [7M]

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