Code No:R2022042 **R20** **SET - 1**

II B. Tech II Semester Supplementary Examinations, December - 2022

DIGITAL IC DESIGN

(Electronics & Communication Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks

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UNIT-I

1	a)	Discuss different data types, data objects in VHDL?	[7M]
	b)	Write the syntax for If statement, Case statement and for Loop.	[7M]
		Or	
2	a)	Write the basic differences between VHDL and VERILOG.	[7M]
	b)	Write different data types used in VERILOG.	[7M]
		UNIT-II	
3	a)	Design binary to gray code converter circuit and write its VHDL code.	[7M]
	b)	Design an 4- bit ALU and write its VHDL code.	[7M]
		Or	
4	a)	Design BCD adder and write its VHDL code.	[7M]
	b)	Design a 2 bit comparator and write its VHDL code.	[7M]
		UNIT-III	
5	a)	Design a 4 bit up-down counter using IC and explain its operation.	[7M]
	b)	Design an universal shift register using IC and discuss different states.	[7M]
		Or	
6	a)	What is register? Listout the applications of shift register?	[7M]
	b)	Design a 4 bit ripple counter using IC and explain its operation.	[7M]
		UNIT-IV	
7	a)	Design and discuss the operation of AND gate using depletion nMOS loads.	[7M]
	b)	Design EXOR gate using pass transistor logic.	[7M]
		Or	
8	a)	Design full adder using CMOS.	[10M]
	b)	Discuss the advantages of a transmission gate and explain its application as a switch.	[4M]
		UNIT-V	
9		Design and discuss clocked SR latch, clocked JK latch using CMOS.	[14M]
		Or	
10	a)	Design and discuss D-flip flop using a CMOS.	[7M]
	b)	Design and discuss master slave JK latch using CMOS.	[7M]

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