Code No: R1922023 **R19** SET - 1

II B. Tech II Semester Regular Examinations, August/September - 2021
DIGITAL ELECTRONICS
(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions each Question from each unit
All Questions carry **Equal** Marks
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1	a)	Given the two binary numbers X = 1010101 and Y = 1001011, perform the subtraction X-Y using 1's and 2's complements.	[8M]
	b)	Given the Boolean function: F=xy+x'y'+y'z (i) Implement it with only OR and NOT gates. (ii) Implement it with only AND and NOT gates.	[7M]
		Or	
2	a)	Convert $(347)_{10}$ into $(\ )_2$, $(\ )_8$, $(\ )_5$ $(\ )_{16}$, and $(\ )_{BCD.}$	[8M]
	b)	Realize 2 input X-OR gate and 2 input X-NOR gates using NAND gates only.	[7M]
3	a)	Simplify the following Boolean expressions by manipulation of Boolean algebra. 1. F(x,y,z)=xy+xyz+xyz'+x'yz 2. F(A,B,C,D)=A'C(A'BD)'+A'BC'D'+AB'C	[8M]
	b)	Simplify the following function using Karnaugh maps f(x, y, w, z) = Σ m (0, 1, 2, 3, 7, 8, 10) + Σ d (5, 6, 11, 15), where d represents the don't-care condition.	[7M]
		Or	
4	a)	Define duality principle and explain it with the help of example. Find the complements of the functions F1 = x'yz' + x'y'z and F2 = x(y'z'+yz) by taking their duals and complementing each literal.	[7M]
	b)	What is the significance of tabular minimization? Simplify the function F(A,B,C,D,E)=Σm(0,2,4,6,9,11,13,15) using tabular minimization.	[8M]
5	a)	Design Half adder and full adder using gates.	[8M]
	b)	Implement the following function with a multiplexer: F (A, B, C) =∑m (0, 2, 4, 7).	[7M]
		Or	
6	a)	Obtain an 8×1 multiplexer with a dual 4-line to 1-line multiplexers having separate enable inputs but common selection lines.	[7M]
	b)	design a BCD-to-Seven segment decoder.	[8M]
7	a)	Explain clocked RS flip flop with the help of logic diagram and truth table.	[7M]
	b)	Design a Mod 7 binary counter. Draw its state diagram and circuit.	[8M]
		Or	
8	a)	Explain clocked D flip flop with NAND gates only? Define the working of D flip flop with truth table.	[7M]
	b)	Design 3-bit binary counter using T flip-flop.	[8M]
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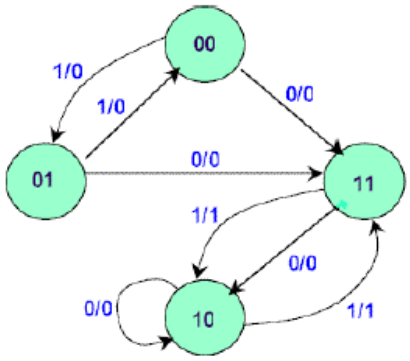
9 a) Distinguish between Mealy and Moore Machines. [7M]

b) Give the state table for the given state diagram. Also give the state assignment [8M]



Or

10 a) What is meant by State Reduction? Explain Partitioning Method of State Reduction. [7M]

b) For the given Moore machine transition table Convert into Mealy machine. [8M]

Present State	Next State		Output
	a = 0	a = 1	
q0	q3	q1	1
q1	q0	q3	0
q2	q2	q2	0
q3	q1	q0	1