Code No: R2022022 **R20** **SET - 1**

II B. Tech II Semester Supplementary Examinations, December - 2022

DIGITAL ELECTRONICS

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 70**

Answer any **FIVE** Questions, each Question from each unit

All Questions carry **Equal** Marks

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UNIT-I

1 a) State and Explain the DeMorgan's Theorem and Consensus Theorem [7M]

b) Realize 2 input X-OR and X-NOR gates using only NOR gates and only NAND gates [7M]

Or

2 a) Convert the following numbers [8M]

i) $(615)_{10} = (\ )_{16}$

ii) $(214)_{16} = (\ )_{8}$

iii) $(0.8125)_{10} = (\ )_{2}$

iv) $(658.825)_{10} = (\ )_{4}$

b) Express the Boolean function F(p, q, r, s)=s(p'+q)+q's in a sum of minterms and a product of maxterms. [6M]

UNIT-II

3 a) Perform BCD addition and Excess-3 addition for the following numbers 0001 0011 and 0010 0110. [6M]

b) With a neat diagram, explain in detail about the working of a 4 bit look ahead adder. Also mention its advantages over conventional adder. [8M]

Or

4 a) Simplify the Boolean function F(A,B,C,D)=Σm(0,2,3,7,11,12,14,15) using tabulation method. [7M]

b) Explain full- Adder. Implement a full- Adder using half Adders. [7M]

UNIT-III

5 a) Obtain an 8×1 multiplexer with a dual 4-line to 1-line multiplexers having separate enable inputs but common selection lines. Use block diagram construction. [7M]

b) Design a 4-bit magnitude comparator with three outputs : A>B, A=B, A<B [7M]

Or

6 a) Design BCD to grey code converter and draw the logic diagram. [7M]

b) Use PLA with 3 inputs, 4 AND terms and two outputs to implement the following Boolean functions F1(A,B,C)= ∑m(3,5,6,7) and F2(A,B,C)= ∑m(1,2,3,4) [7M]

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UNIT-IV

7 a) Realize JK Flip flop using SR Flip flop and derive their characteristic equations. [7M]

b) Design 4-bit Asynchronous counter using JK flip flop with its timing diagram. [7M]

Or

8 a) Write difference between Combinational & Sequential circuits. [7M]

b) Build a 4bit universal shift register using D flipflops and multiplexers. [7M]

UNIT-V

9 a) Design 4-stage twisted ring counter with circuit diagram, state transition diagram and state table. [7M]

b) A clocked sequential circuit with single input x and single output z produces output z=1, whenever the input x completes the sequence 1011 and overlapping is allowed: i) Obtain the state diagram ii) Obtain its minimum state table and design circuit with D flip flop. [7M]

Or

10 a) Explain capabilities and limitations of finite state machine. [7M]

b) Draw state diagram in Mealy model for the following state table. [7M]

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
A	A	C	0	1
B	D	A	0	0
C	C	A	1	0
D	B	D	1	0