Time: 3 hours

Max. Marks: 70

## II B. Tech II Semester Regular/Supplementary Examinations, November - 2020 COMPUTER ORGANIZATION

(Com to CSE, IT, ECC)

Note: 1. Question Paper consists of two parts (Part-A and Part-B) 2. Answer ALL the question in Part-A 3. Answer any **FOUR** Questions from **Part-B** PART -A (2M)1. a) Differentiate multi computers and multi processors. (2M)Define the terms instruction code and operation code. (2M)Describe the different types of DRAMS. (2M)Write about memory hierarchy in computer system? (3M)Explain with example the implementation of register transfer? (3M)Write sequence of micro-operations for the fetch cycle of basic computer. PART -B (7M) 2. Design a bus system for interconnecting four n bit registers b) Design a 4-bit arithmetic circuit which implements addition, subtraction, (7M) Increment and decrement operations. (7M)Differentiate relative and absolute addressing modes for branch instructions. b) Describe, with proper examples, the role of processor stack in subroutine call (7M) and return. a) Design an adder/subtractor circuit with one selection variable s and two inputs (7M) A and B. When s=0, the circuit performs A+B and when s=1 it performs A-B, by taking 2's complement of B. b) List the different type of Arithmetic and logic Instruction with suitable (7M)examples. 5. a) (7M)Differentiate between Synchronous Bus, Asynchronous bus, Interface Circuits. b) Explain briefly about Direct memory Access. Why does DMA have Priority (7M)over the CPU when both request a memory transfer? 6. a) Compare and contrast between Asynchronous DRAM and Synchronous (7M) DRAM. b) Define Virtual Memory. Explain the process of converting virtual addresses to (7M)physical addresses with a neat diagram. 7. a) Draw the block diagram of microprogram sequencer for a control Memory and (7M)explain. b) Explain the design of a 4bit Arithmetic unit with two selection variables, which (7M)performs the basic arithmetic functions.