III B. Tech I Semester Supplementary Examinations, June/July-2022
COMPILER DESIGN
(Computer Science and Engineering)

Time: 3 hours　　　　　　　　　　　　　　　　　　　　Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1.　a)　With neat diagram explain different phases of compiler. Mention the input and output of each phase　[8M]

　　b)　Derive the regular expression for the tokens given below and also draw a transition diagram to recognize the following tokens:　[7M]
　　　　i)　Relational operators
　　　　ii)　Integer constant
　　　　iii)　Identifier
　　　　iv)　White spaces
　　　　v)　Exponent part of a number

(OR)

2.　a)　Explain in detail about LEX tool.　[8M]

　　b)　Write the steps to convert Non-Deterministic Finite Automata (NDFA) into Deterministic Finite Automata (DFA).　[7M]

UNIT-II

3.　a)　Write the properties of LR parser with its structure. Also explain the techniques of LR parser.　[8M]

　　b)　What is Left Recursion? How to eliminate Left Recursion.　[7M]

(OR)

4.　a)　Construct predictive parser for the following grammar:　[8M]
　　　　S-->(L)/a
　　　　L-->L,S/S and parse any input string.

　　b)　Describe the Error recovery scheme in YACC.　[7M]

UNIT-III

5.　a)　What is symbol table? Explain how the hash table is used to construct a symbol table.　[8M]

　　b)　What are the reasons to use intermediate code in a compiler? Write the intermediate code for the expression a + a * (b + c) * d.　[7M]

(OR)

6.　a)　What are the contents of a symbol table? Explain in detail about the symbol table organization for block structured languages.　[8M]

　　b)　Write down the translation procedure for control statement?　[7M]

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UNIT-IV

7. a) Compare static versus dynamic memory allocation. [8M]
    b) Describe in detail about stack allocation of space and heap management. [7M]

(OR)

8. a) Explain Storage allocation strategies with suitable examples? [8M]
    b) Illustrate the mechanism of elimination of partial redundancy in data flow analysis. [7M]

UNIT-V

9. a) What are the properties of code generation phase? Also explain the Design Issues of this phase. [8M]
    b) Explain the target machine architecture? [7M]

(OR)

10. a) What are basic blocks? Write the algorithm for partitioning into Blocks. [8M]
    b) Explain the simple code generator and generate target code sequence for the following statement d:=(a-b)+(a-c)+(a-c). [7M]

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