

# III B. Tech I Semester Regular Examinations, Dec/Jan -2022-23 ANALOG ICs AND APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 70

#### Answer any **FIVE** Questions **ONE** Question from **Each unit** All Questions Carry Equal Marks

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# <u>UNIT-I</u>

- 1. a) What is an operational amplifier? Give its symbol and also draw [7M] its electrical equivalent circuit.
  - b) Compare ideal and practical OP-AMP parameters. [7M]

#### (OR)

- 2. a) Define the terms: SVRR, Input bias current, Input offset voltage, [7M] Gain bandwidth product.
  - b) Explain the IC 741 op-amp block diagram & its features in [7M] detail.

#### UNIT-II

- 3. a) What are the advantages of instrumentation amplifier? Derive an [7M] expression for the transfer function of an instrumentation amplifier.
  - b) For the non-inverting a.c amplifier  $R_{in} = 50 \ \Omega$ ,  $C_i = 0.1 \ \mu\text{F}$ , [7M]  $R_1 = 100 \ \Omega$ ,  $R_F = 1k\Omega$  and  $R_O = 10 \ k\Omega$ . Determine the gain and band width of the amplifier.

### (OR)

- 4. a) What are the different modes of operation of an active [7M] integrator? Explain
  - b) Design a practical integrator circuit to process the sinusoidal [7M] input waveform upto 1 kHz and the input amplitude is 10 mV. Assume necessary standard values of resistance.

# UNIT-III

- 5. a) Draw the op-amp circuit configuration of a band-pass filter [7M] formed by cascading two pole high-pass filters and a two pole low-pass filter, and derive the expression for centre frequency f<sub>0</sub>.
  - b) Design a second order Butter-worth low pass filter having a cut- [7M] off frequency of 1 kHz. The damping factor is equal to 1.414.

# (OR)

- 6. a) Design a Band Pass filter with fc =1 kHz, Q=3 and  $A_f$  =10. Draw [7M] the circuit with all the components.
  - b) Explain the Narrow-Band –Reject filter with the help of a circuit [7M] diagram.

# UNIT-IV

- 7. a) Draw the pin diagram of 566 VCO IC and list important [7M] specifications of 566 VCO IC.
  - b) Design an Astable multivibrator having an output frequency 15 [7M] KHz with duty cycle of 40%.

#### (OR) 1 of 2

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# **R20**

- 8. a) With the help of neat diagrams explain the operation of Schmitt [7M] trigger using 555 timer.
  - b) Derive an expression for the lock-in range of a PLL. [7M]

UNIT-V

- 9. a) Draw the block diagram of inverted R-2R DAC and explain its [7M] operation in detail.
  - b) List out the DAC and ADC Specifications and compare them in [7M] detail.

(OR)

- 10. a) Explain the specifications of DAC & ADC with an example. [7M]
  - b) Find the voltage at all nodes 0, 1, 2 ..., and at the output of a [7M] 5-bit R-2R ladder DAC. The LSB is 1 and all other bits are equal to '0'. Assume  $V_R$  = -10V and R = 10k $\Omega$ .

2 of 2





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# UNIT-I

- 1. a) Draw the IC 741 op-amp pin diagram and explain the function of [7M] each pin in detail.
  - b) Discuss briefly about the DC characteristics of an operational [7M] amplifier?

# (OR)

- 2. a) Name the most important parameters of an operational [7M] amplifier. What are their ideal values and practical values?
  - b) What is a voltage regulator? Explain the three-terminal voltage [7M] regulator with the help of block diagram?

# UNIT-II

- 3. a) Explain the operation of a practical differentiator. Use relevant [7M] expressions, diagrams.
  - b) Draw the circuit of a voltage to current converter if the load is [7M] floating and grounded. Are there any limitations as the size of the load when grounded?

# (OR)

- 4. a) Using three op-amps draw the circuit diagram of an [7M] instrumentation amplifier and derive an expression for the output voltage?
  - b) Design a single op-amp logarithmic amplifier and derive the [7M] relation between the output and input voltage to explain why it is called a logarithmic amplifier?

# <u>UNIT-III</u>

5. a) Plot and explain frequency response of [7M] i) Low pass filter ii) High pass filter

iii) Band pass filter iv) Band Reject filter

b) With neat circuit diagram explain the operation of 2<sup>nd</sup> order [7M] butter worth HPF and derive an expression for voltage gain.

# (OR)

- 6. a) With suitable circuit diagram explain the operation of 2<sup>nd</sup> order [7M] band reject filter.
  - b) Design a low pass filter with a cutoff frequency of 1kHz and with [7M] a pass band gain of 2.

# UNIT-IV

- 7. a) Give the circuit of monostable multivibrator with 555 timer, [7M] explain its operation by deriving expression for pulse width.
  - b) Draw the block diagram of NE/SE565 PLL and explain the [7M] operation with the help of waveforms.

(OR)

|'''|'|'|'||

# (R20)

# ( SET - 2 )

- 8. a) Explain Astable multivibrator circuit using 555.Also derive [7M] expression for time period.
  - b) What is meant by VCO? Explain in detail and state the [7M] applications of VCO?

#### UNIT-V

- 9. a) Define the following terms [7M] i) Accuracy ii) Resolution iii) Conversion time iv) Percentage resolution
  - b) Draw the circuit of a ladder type DAC for 4 bits and derive [7M] expression for output voltage.

- 10. a) Which type of DAC is more preferable? Draw the circuit diagram [7M] and obtain expression for output voltage for 4-bits?
  - b) Draw the schematic circuit diagram of dual-slope A/D converter [7M] and explain its operation. Derive expression for output voltage.

Code No: R2031041





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# UNIT-I

- 1. a) What is an Op-Amp? Draw the functional block diagram of an [7M] Op-Amp and explain each block in detail.
  - b) List out the AC characteristics of an op-amp and discuss about [7M] them?

(OR)

- 2. a) Define the terms: [7M] CMRR, PSRR, SVRR, Input bias current, Input offset voltage, Gain bandwidth product.
  - b) For an OP-AMP, PSRR is 70dB, CMRR is 10<sup>5</sup>, and differential [7M] mode gain is 10<sup>5</sup>. The output voltage changes by 20V in 4 µsec. Calculate: (i) numerical value of PSRR (ii) Common mode gain (iii) Slew rate.

# UNIT-II

- 3. a) Draw the circuit of an op-amp integrator and derive the output [7M] expression.
  - b) Draw and explain the operation of a square wave generator. [7M]

(OR)

- 4. a) Construct a logarithmic amplifier with op-amp and derive the [7M] expression for the output voltage.
  - b) Draw the circuit diagram of a monostable multivibrator using [7M] op-amp, derive the expression for its frequency of oscillation.

# UNIT-III

- 5. a) Design a first order band pass filter with lower cutoff frequency [7M] of 100Hz and a higher cutoff frequency of 1KHz. The pass band gain should be 4. Calculate the 'Q' of the filter.
  - b) Write brief notes on band pass, band reject and all pass filters. [7M]

# (OR)

- 6. a) With suitable circuit diagram explain the operation of Narrow [7M] band pass filter (NBPF) and give the necessary design expression.
  - b) Using an op-amp, design a second order low-pass filter with a [7M] cutoff frequency of 1KHz.

# <u>UNIT-IV</u>

- 7. a) Draw the circuit of a Schmitt trigger using 555 timer and explain [7M] its operation.
  - b) What are the modes of operation of IC555? Derive the expression [7M] of time delay of a monostable multivibrator.

|'''|'|'|'||

Code No: R2031041

# **SET - 3**

- 8. a) Explain the functional diagram of a 555 Timer with neat sketch. [7M]
  - b) With the help of block diagram explain the operation of a voltage [7M] controlled oscillator.

# <u>UNIT-V</u>

- 9. a) Describe the principle of working of an R-2R DAC. What are the [7M] minimum and maximum values of gain for it? How can a DAC be used as current-to-voltage converter?
  - b) Draw and explain the block diagram of a counter type ADC and [7M] list out its disadvantages.

- 10. a) Draw the simplified block diagram of a successive approximation [7M] ADC and explain its working.
  - b) Draw the circuit diagram of 5-bit inverted R-2R ladder DAC. How [7M] many levels are possible in this DAC? What is its resolution if the output range is 0 to 10 V.





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# <u>UNIT-I</u>

- 1. a) Derive CMRR of emitter coupled differential amplifier. What do [7M] you mean by difference mode gain?
  - b) Mention the types of open loop configurations of an Op-Amp. [7M] Explain each configuration in detail.

#### (OR)

- 2. a) Define slew rate of an Op-amp and explain its significance in the [7M] dynamic characteristics of an Op-amp.
  - b) An op-amp has a slew rate of  $2V/\mu s$ . What is the maximum [7M] frequency of an output sinusoid of peak value 5V at which the distortion sets in due to the slew rate limitation?

# <u>UNIT-II</u>

- 3. a) Draw the circuit of an ideal integrator and explain its operation. [7M] What are the limitations of an ideal integrator? How these limitations can be overcome?
  - b) Design and explain triangular wave generator using Schmitt [7M] trigger and integrator circuit.

# (OR)

- 4. a) Draw and explain non-inverting comparator and its input and [7M] output wave forms i) if Vref is Positive ii) if Vref is Negative.
  - b) Design a differentiator to differentiate an input signal that varies [7M] in frequency from 100Hz to 10KHz. If a sine wave of 1.2V Peak at 10KHz is applied to the differentiator of part, draw its output wave form.

# UNIT-III

- 5. a) Draw a band pass filter circuit with its frequency response [7M] curve. Explain its working.
  - b) Design a second order high pass filter with a cutoff frequency of [7M] 2 kHz.

- 6. a) Describe the principle of operation of an inverting first order low- [7M] pass filter using op-amp and draw its frequency response curve?
  - b) Design a wide band-pass filter with  $f_L=200Hz$ ,  $f_H=1kHz$  and a [7M] pass band gain=4. Draw the frequency response and calculate 'Q' factor for the filter.



# SET - 4

# UNIT-IV

- 7. a) Draw the dc voltage versus phase difference characteristic of [7M] balanced modulator phase detector of a PLL indicating all important regions.
  - b) With a neat functional diagram, explain the operation of VCO [7M] and also derive an expression for free running frequency,  $f_0$ .

#### (OR)

- 8. a) Draw the circuit diagram of a 555 timer connected as an astable [7M] multivibrator and explain its operation?
  - b) Using 555 timers, design a monostable multivibrator to produce [7M] pulses of width 110 msec. Use a 1µF capacitor?

# UNIT-V

- 9. a) Using a neat sketch, explain the working of a parallel [7M] comparator ADC?
  - b) Draw the circuit of a Weighted Resistor DAC and obtain [7M] expression for n-bits.

- 10. a) Explain R-2R ladder DAC for 4-bit operation. The resolution of [7M] this DAC is 1mv. If 0000 represents 0 V, determine the output for an input of 1010.
  - b) Explain the operation of Dual-slope ADC with functional [7M] diagram.